Digital Logic Lab 5 Report

Digital Logic 2116L

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Featheringill 210

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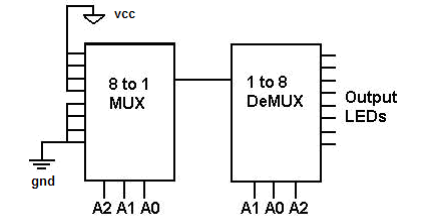
1. Introduction:

The basic concepts we learned for this lab how to save an existing schematic and use it in another schematic. We learned to build 8-to-1 Mux, 1-to-8 Demux, 4 bits adder, etc.

1. Design Requirements:

We need to design the part 2 circuit using our pre-build Mux and Demux gate in lab.

1. Diagrams



1. Results

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A0 | A1 | A2 | O0 | O1 | O2 | O3 | O4 | O5 | O6 | O7 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Discussion

Everything in the lab runs smoothly, we did the prelab and the implementation process to the board took little time

1. Conclusion

I learned how reuse schematic in Quartz II and the general idea of reusability

1. Post-Lab Questions

I think the time when it’s least useful is that we are required to build a specific circuit that only serves the purpose of one thing instead of more generic. For instance the circuit we built for Part 2 seems not so useful if exported to a symbol.